

DATA SHEET

TDA4566

Colour transient improvement
circuit

Preliminary specification
File under Integrated Circuits, IC02

March 1991

Colour transient improvement circuit

TDA4566

GENERAL DESCRIPTION

The TDA4566 is a monolithic integrated circuit for colour-transient improvement (CTI) and luminance delay line in gyrator technique in colour television receivers.

Features

- Colour transient improvement for colour difference signals (R-Y) and (B-Y) with transient detecting-, storage- and switching stages resulting in high transients of colour difference output signals
- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 550 ns to 820 ns in steps of 90 ns and additional fine adjustment of 37 ns
- Two Y output signals; one of 180 ns less delay

QUICK REFERENCE DATA

| PARAMETER | CONDITIONS | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---------------|------|------|------|------|
| Supply voltage (pin 10) | | V_P | 10.8 | 12 | 13.2 | V |
| Supply current (pin 10) | | I_P | – | 35 | 50 | mA |
| Y-signal delay at pin 12 | S1 open; $R_{14-18} = 1.2 \text{ k}\Omega$; note 1 | | | | | |
| $V_{15-18} = 0 \text{ to } 2.5 \text{ V}$ | | t_{17-12} | 490 | 550 | 610 | ns |
| $V_{15-18} = 3.5 \text{ to } 5.5 \text{ V}$ | | t_{17-12} | 580 | 640 | 700 | ns |
| $V_{15-18} = 6.5 \text{ to } 8.5 \text{ V}$ | | t_{17-12} | 670 | 730 | 790 | ns |
| $V_{15-18} = 9.5 \text{ to } 12 \text{ V}$ | | t_{17-12} | 760 | 820 | 880 | ns |
| Y-signal amplification (R-Y) and (B-Y) signal attenuation | 0.5 MHz | α_Y | 0 | 1 | 2 | dB |
| output transient time | | α_{cd} | –1 | 0 | +1 | dB |
| | | t_{tr} | – | 100 | 200 | ns |

Note

1. Delay time is proportional to resistor R_{14-18} .
 R_{14-18} also influences the bandwidth; a value of 1.2 k Ω results in a bandwidth of 5 MHz (typ.).

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102); SOT102-1; 1996 November 27.

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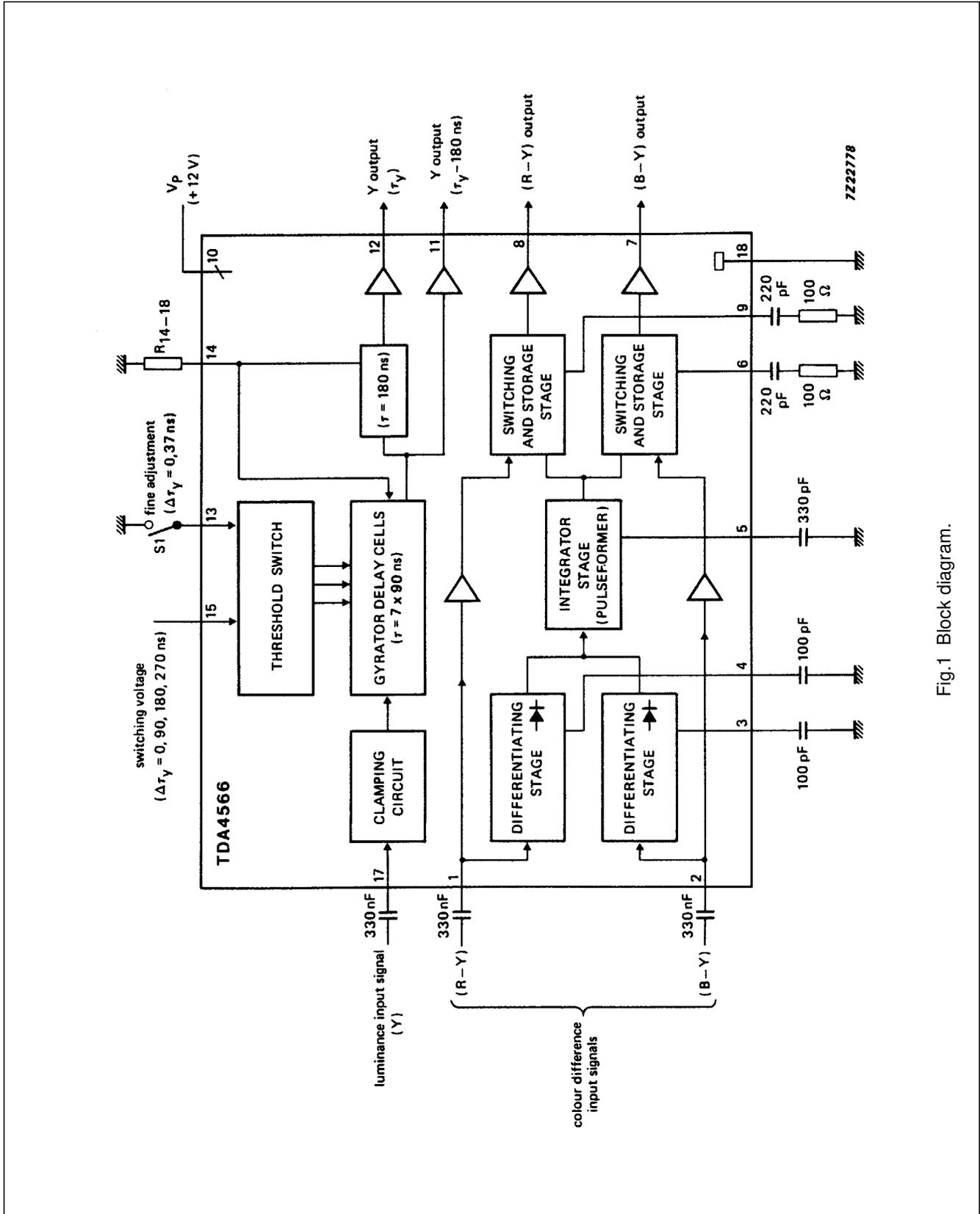


Fig.1 Block diagram.

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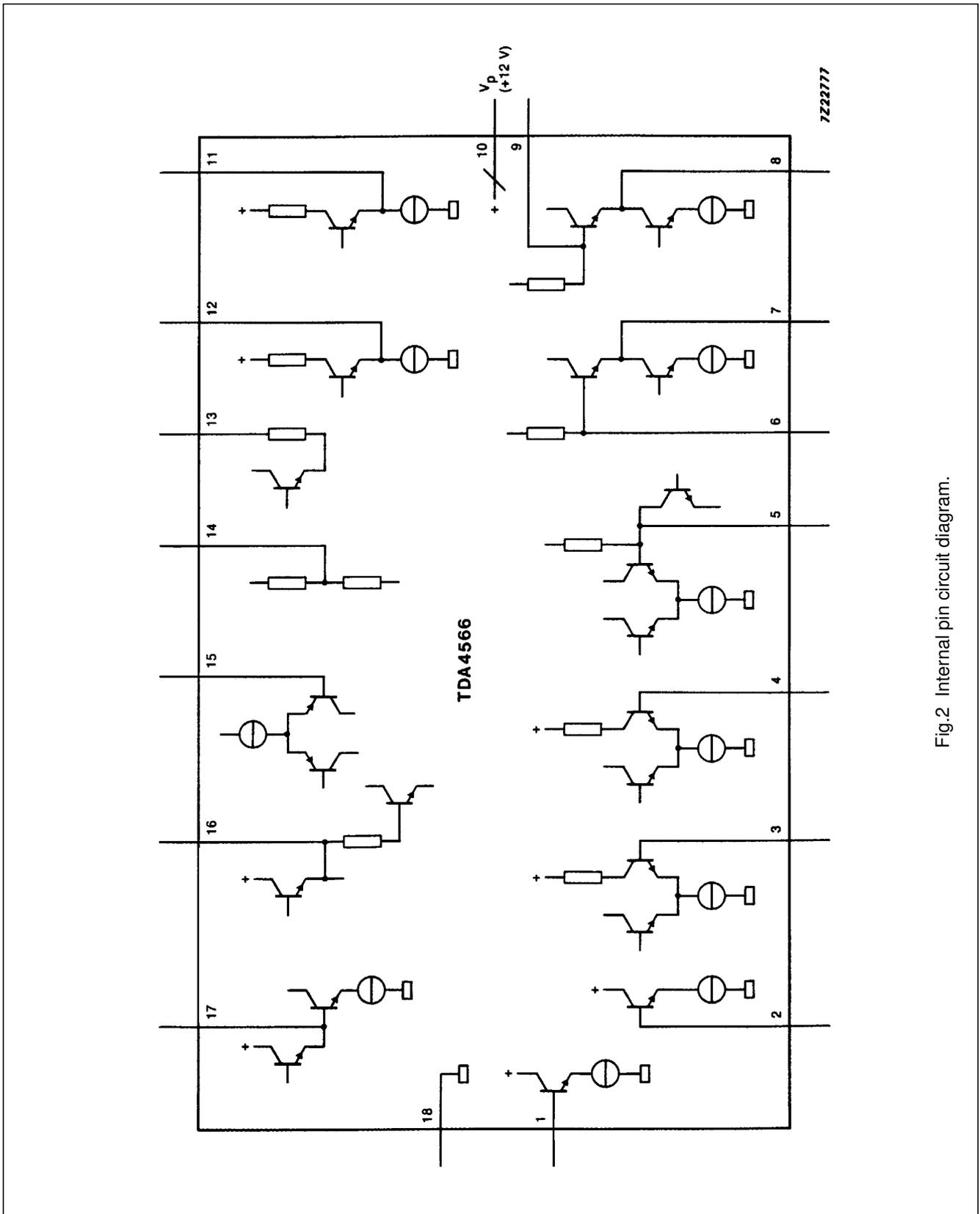


Fig.2 Internal pin circuit diagram.

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|-------------------|------|-----------------------|------------------|
| Supply voltage range (pin 10) | $V_P = V_{10-18}$ | 0 | 13.2 | V |
| Voltage ranges to pin 18 (ground) | | | | |
| at pins 1, 2, 12 and 15 | V_{n-18} | 0 | V_P | V |
| at pin 11 | V_{11-18} | 0 | $(V_P - 3 \text{ V})$ | V |
| at pin 17 | V_{17-18} | 0 | 7 | V |
| Voltage ranges | | | | |
| at pin 7 to pin 6 | V_{7-6} | 0 | 5 | V |
| at pin 8 to pin 9 | V_{8-9} | 0 | 5 | V |
| Currents | | | | |
| at pins 6, 9 | $I_{6,9}$ | -10 | +10 | mA |
| at pins 7, 8, 11 and 12 | $I_{7,8,11,12}$ | | internally limited | |
| Total power dissipation ($T_j = 150 \text{ }^\circ\text{C}$; $T_{amb} = 70 \text{ }^\circ\text{C}$) | P_{tot} | - | 1.1 | W |
| Storage temperature range | T_{stg} | -25 | +150 | $^\circ\text{C}$ |
| Operating ambient temperature range | T_{amb} | 0 | +70 | $^\circ\text{C}$ |

THERMAL RESISTANCE

From junction to ambient (in free air)

$$R_{th\ j-a} = 70 \text{ K/W}$$

Note

1. Pins 3, 4, 5, 6, 9, 13 and 14 DC potential not published.

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CHARACTERISTICS $V_P = V_{10-18} = 12\text{ V}$; $T_{\text{amb}} = 25\text{ °C}$; measured in application circuit Fig.3; unless otherwise specified

| PARAMETER | CONDITIONS | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|--|------------|--------------|------|------|------|------------|
| Supply (pin 10) | | | | | | |
| Supply voltage | | V_P | 10.8 | 12 | 13.2 | V |
| Supply current | | I_P | – | 35 | 50 | mA |
| Colour difference paths | | | | | | |
| (R-Y) input voltage (75% colour bar signal) (peak-to-peak value) | | $V_{1(p-p)}$ | – | 0.63 | 1.5 | V |
| (B-Y) input voltage (75% colour bar signal) (peak-to-peak value) | | $V_{2(p-p)}$ | – | 0.8 | 1.9 | V |
| Input resistance | | | | | | |
| (R-Y) | | R_{1-18} | 8 | 12 | 16 | k Ω |
| (B-Y) | | R_{2-18} | 8 | 12 | 16 | k Ω |
| Internal bias voltage | | | | | | |
| (R-Y) | | V_{1-18} | 3.8 | 4.3 | 4.8 | V |
| (B-Y) | | V_{1-18} | 3.8 | 4.3 | 4.8 | V |
| Signal attenuation | | | | | | |
| (R-Y) | | V_8 / V_1 | –1 | 0 | + 1 | dB |
| (B-Y) | | V_7 / V_2 | –1 | 0 | + 1 | dB |
| Output transient time | note 1 | t_{tr} | – | 100 | 200 | ns |
| Output resistance | | | | | | |
| (B-Y) | | R_{7-18} | – | 100 | – | Ω |
| (R-Y) | | R_{8-18} | – | 100 | – | Ω |
| DC output voltage | | | | | | |
| (B-Y) | | V_{7-18} | 3.8 | 4.3 | 4.8 | V |
| (R-Y) | | V_{8-18} | 3.8 | 4.3 | 4.8 | V |
| Output current | | | | | | |
| source | note 2 | $I_{7,8}$ | 0.4 | – | – | mA |
| sink | | $-I_{7,8}$ | 1.0 | – | – | mA |

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| PARAMETER | CONDITIONS | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|------|-------|------|-----------------|
| Y-signal path | | | | | | |
| Y-input voltage (composite signal) (peak-to-peak value) | capacitive coupling | $V_{17(p-p)}$ | – | 0.45 | 0.62 | V |
| Internal bias voltage | during clamping | V_{17-18} | 2.1 | 2.4 | 2.7 | V |
| Input current | | | | | | |
| during picture content | | I_{17} | – | 8 | 12 | μA |
| during sync. pulse | | $-I_{17}$ | – | 100 | 150 | μA |
| Y-signal delay at pin 12 | S1 open; $R_{14} = 1.2 \text{ k}\Omega$; notes 3 and 4 | | | | | |
| at $V_{15-18} = 0$ to 2.5 V | | t_{17-18} | 490 | 550 | 610 | ns |
| at $V_{15-18} = 3.5$ to 5.5 V | | t_{17-18} | 580 | 640 | 700 | ns |
| at $V_{15-18} = 6.5$ to 8.5 V | | t_{17-18} | 670 | 730 | 790 | ns |
| at $V_{15-18} = 9.5$ to 12 V | | t_{17-18} | 760 | 820 | 880 | ns |
| Fine adjustment of Y-signal delay for all 4 steps | S1 closed | t_{17-12} | – | 37 | – | ns |
| Signal delay between pin 11 and pin 12 | S1 open | t_{11-12} | 160 | 180 | 200 | ns |
| Dependency of delay time on temperature | | $\frac{\Delta t_{17-12}}{t_{17-12} \cdot \Delta T_j}$ | – | 0.001 | – | K^{-1} |
| on supply voltage | | $\frac{\Delta t_{17-12}}{t_{17-12} \cdot \Delta V_P}$ | – | –0.03 | – | V^{-1} |
| Input switching current | | $-I_{15}$ | – | 15 | 25 | μA |
| Y-signal attenuation | $f = 0.5 \text{ MHz}$ | | | | | |
| pin 11 from pin 17 | | V_{11}/V_{17} | –1 | 0 | +1 | dB |
| pin 12 from pin 17 | | V_{12}/V_{17} | 0 | +1 | +2 | dB |
| Frequency response at 3 MHz referred to 0.5 MHz | note 5 | | | | | |
| pin 11 | | $\frac{V_{11}(3 \text{ MHz})}{V_{11}(0.5 \text{ MHz})}$ | 0 | – | 3.0 | dB |
| pin 12 | | $\frac{V_{12}(3 \text{ MHz})}{V_{12}(0.5 \text{ MHz})}$ | 0 | – | 3.0 | dB |

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| PARAMETER | CONDITIONS | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|--|------------|---|------|------|------|------|
| Frequency response at 5 MHz referred to 0.5 MHz pin 11 | note 5 | $\frac{V_{11}(5 \text{ MHz})}{V_{11}(0.5 \text{ MHz})}$ | -3.0 | - | 2.0 | dB |
| pin 12 | | $\frac{V_{12}(5 \text{ MHz})}{V_{12}(0.5 \text{ MHz})}$ | -3.0 | - | 2.0 | dB |
| DC output voltage pin 11 | | V_{11-18} | 1.8 | 2.3 | 2.6 | V |
| pin 12 | | V_{12-18} | 9.8 | 10.3 | 10.8 | V |
| Output current | note 2 | | | | | |
| source | | $I_{11, 12}$ | - | - | 0.4 | mA |
| sink | | $-I_{11, 12}$ | - | - | 1.0 | mA |

Notes

1. Output signal transient time measured with $C_{6-18} = C_{9-18} = 220 \text{ pF}$ without resistor (see Fig. 3).
2. Output current measured with emitter follower with constant current source of 0.6 mA.
3. R_{14-18} influences the bandwidth; a value of 1.2 k Ω results in a bandwidth of 5 MHz (typ.).
4. Delay time is proportional to resistor R_{14-18} . Devices with suffix "A" require the value of the resistor to be 1.15 k Ω ; a 27 k Ω ; resistor connected in parallel with $R_{14-18} = 1.2 \text{ k}\Omega$;
5. Frequency response measured with $V_{15-18} = 9.5 \text{ V}$ and switch S1 open.

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APPLICATION INFORMATION

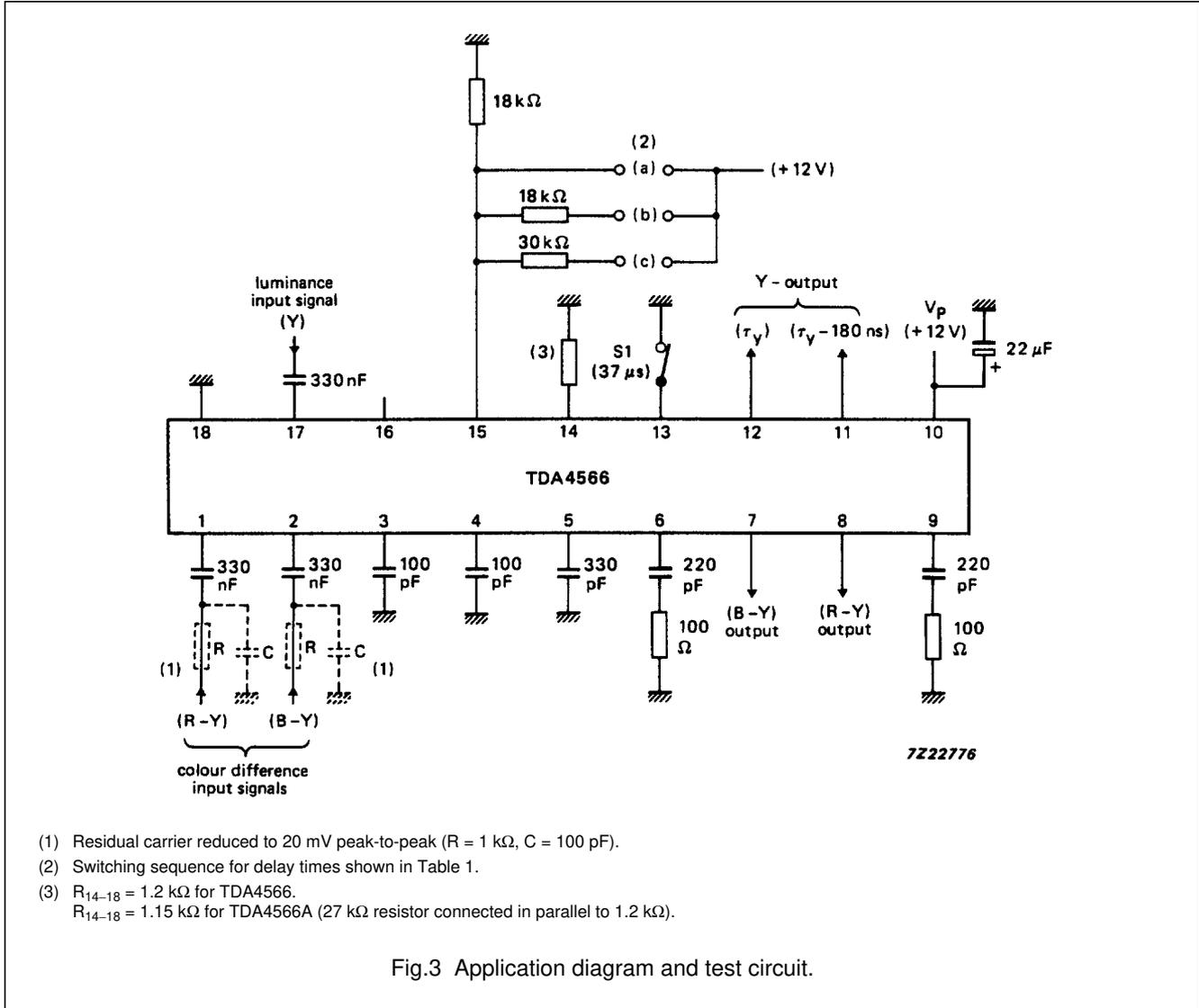


Table 1 Switching sequence for delay times.

| CONNECTION ⁽²⁾ | | | VOLTAGE AT PIN 15 | DELAY TIME (ns) ⁽¹⁾ |
|---------------------------|-----|-----|-------------------|--------------------------------|
| (a) | (b) | (c) | | |
| 0 | 0 | 0 | 0 to 2.5 V | 550 |
| 0 | 0 | X | 3.5 to 5.5 V | 640 |
| 0 | X | X | 6.5 to 8.5 V | 730 |
| X | X | X | 9.5 to 12 V | 820 |

Notes

1. When switch (S1) is closed the delay time is increased by 37 ns.
2. Where: X = connection closed; 0 = connection open.

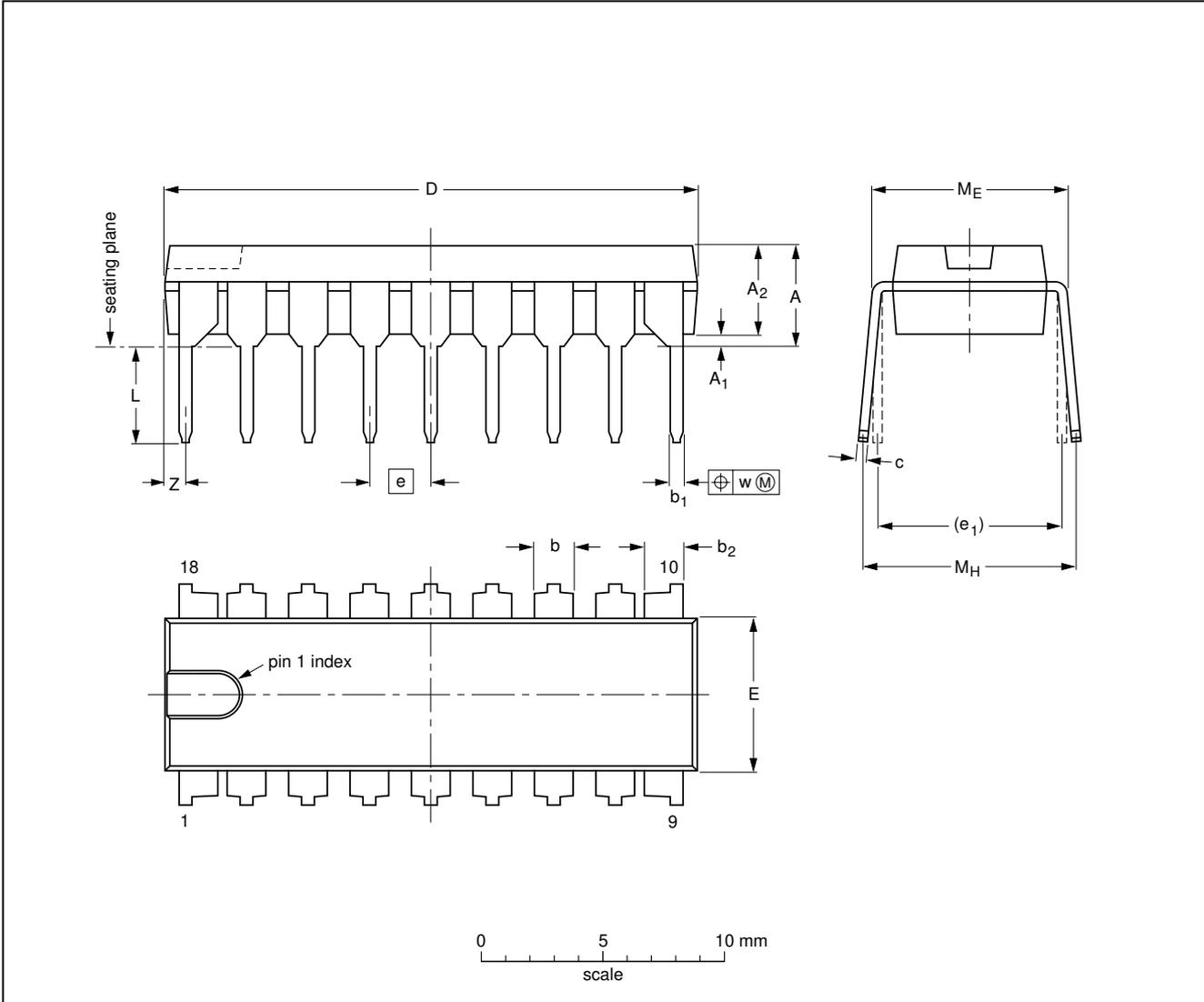
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PACKAGE OUTLINE

DIP18: plastic dual in-line package; 18 leads (300 mil)

SOT102-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | b ₂ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | Z ⁽¹⁾ max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| mm | 4.7 | 0.51 | 3.7 | 1.40 1.14 | 0.53 0.38 | 1.40 1.14 | 0.32 0.23 | 21.8 21.4 | 6.48 6.20 | 2.54 | 7.62 | 3.9 3.4 | 8.25 7.80 | 9.5 8.3 | 0.254 | 0.85 |
| inches | 0.19 | 0.020 | 0.15 | 0.055 0.044 | 0.021 0.015 | 0.055 0.044 | 0.013 0.009 | 0.86 0.84 | 0.26 0.24 | 0.10 | 0.30 | 0.15 0.13 | 0.32 0.31 | 0.37 0.33 | 0.01 | 0.033 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT102-1 | | | | | | 93-10-14 95-01-23 |

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact

with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

| | |
|---|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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